Temperature is becoming the main design constrain:
- Decreases reliability
- Decreases performance
- Increases power consumption
- Increases the chip cost

Chip Multiprocessors already exist:
- The per-core thermal stress is higher.
- But, they offer new ways for dealing with temperature.

Thermal Aware Scheduling (TAS)

Thermal issues on Chip Multiprocessors

CMPs are more “sensitive” to temperature problems.

Thermal Aware Scheduling (TAS) for CMPs

TSIC: Thermal Scheduling Simulator for CMPs

Experimental Results

Optimization 1: Temperature Threshold

Optimization 2: Threshold Neighborhood

Experimental Setup

- CMPs with 4 - 64 cores
- Synthetic workload of 2500 processes
- Average power consumption 10W
- Average lifetime 500 intervals

Thermal Awareness while scheduling significantly improves performance